

CMOS Quad True/Complement Buffer

High Voltage Types (20-Volt Rating)

The RCA-CD4041UB types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041UB is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

The CD4041UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal) -0.5 to +20 V
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5 V
- DC INPUT CURRENT, ANY ONE INPUT ±10 mA
- POWER DISSIPATION PER PACKAGE (P_D):
 - For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 - For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 - For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) 500 mW
 - For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 - For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW
- OPERATING-TEMPERATURE RANGE (T_A):
 - PACKAGE TYPES D, F, K, H -55 to +125°C
 - PACKAGE TYPE E -40 to +85°C
- STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T _A =Full Package-Temperature Range)	3	18	V

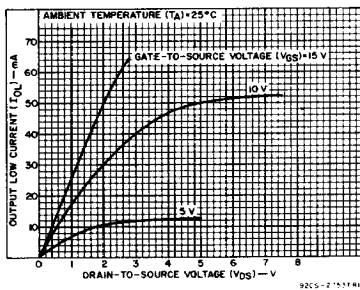


Fig.2 — Typical output low (sink) current characteristics.

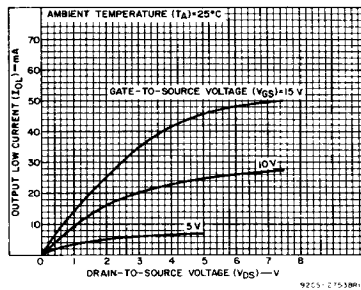


Fig.3 — Minimum low (sink) current characteristics.

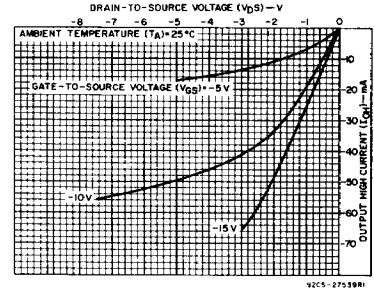


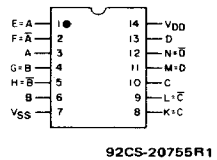
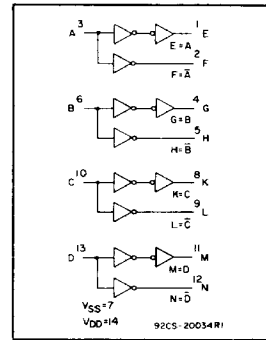
Fig.4 — Typical output high (source) current characteristics.

Features:

- Balanced sink and source current; approximately 4 times standard "B" drive
- Equalized delay to true and complement outputs
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- High current source/sink driver
- CMOS-to-DTL/TTL Converter Buffer
- Display driver
- MOS clock driver
- Resistor network driver (Ladder or weighted R)
- Buffer
- Transmission line driver



TOP VIEW
TERMINAL ASSIGNMENT

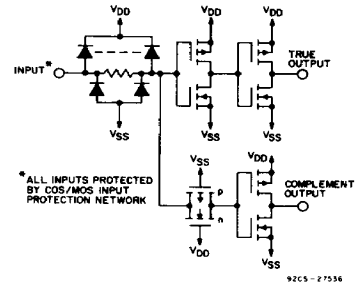


Fig.1 — Schematic diagram 1 of 4 buffers.

CD4041UB Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H, Packages				Values at -40, +25, +85 Apply to E Pkgs.				
				-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current I _{DD} Max.	-	0, 0.10, 0.15, 0.20	5, 10, 15, 20	1, 2, 4, 20	1, 2, 4, 20	30, 60, 120, 600	30, 60, 120, 600	-	0.02	0.02	1, 2, 4, 20	μA
Output Low (Sink) Current, I _{OL} Min.	0.4, 0.5, 1.5	0.5, 0.10, 0.15	5, 10, 15	2.1, 6.25, 24	1.8, 5.6, 23	1.3, 4, 15.5	1.2, 3.5, 13	1.6, 5, 19	3.2, 10, 38	-	-	mA
Output High (Source) Current, I _{OH} Min.	4.6, 2.5, 9.5	0.5, 0.10, 0.15	5, 10, 15	-2.1, -6.25, -24	-1.8, -5.6, -23	-1.3, -4, -15.5	-1.2, -3.5, -13	-1.6, -5, -19	-3.2, -10, -38	-	-	mA
Output Voltage: Low Level, V _{OL} Max.	-	0.5, 0.10, 0.15	5, 10, 15	0.05				-	0	0.05	-	V
Output Voltage: High Level, V _{OH} Min.	-	0.5, 0.10, 0.15	5, 10, 15	4.95, 9.95, 14.95				4.95, 9.95, 14.95	5, 10, 15	-	-	V
Input Low Voltage, V _{IL} Max.	0.5, 1.9, 1.5, 13.5	-	5, 10, 15	1, 2, 2.5				-	-	1, 2, 2.5	-	V
Input High Voltage, V _{IH} Min.	0.5, 1.9, 1.5, 13.5	-	5, 10, 15	4, 8, 12.5				4, 8, 12.5	-	-	-	V
Input Current, I _{IN} Max.	-	0, 0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	-	μA

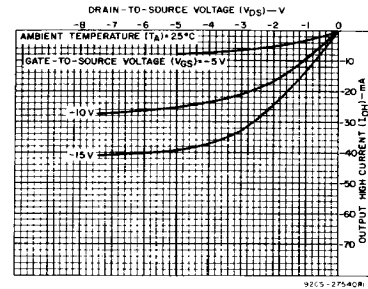


Fig. 5 - Minimum output high (source) current characteristics.

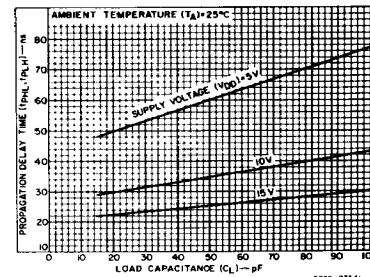


Fig. 6 - Typical propagation delay time vs. load capacitance.

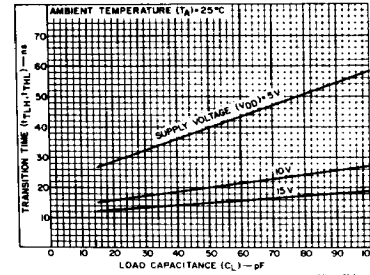


Fig. 7 - Typical transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS	ALL TYPES LIMITS		UNITS	
		V _{DD} Volts	Typ.		Max.
Propagation Delay Time: t _{PHL} , t _{PLH}		5	60	120	ns
		10	35	70	
		15	25	50	
Transition Time: t _{THL} , t _{TLH}		5	40	80	ns
		10	20	40	
		15	15	30	
Input Capacitance C _{IN}	Any Input	15	22.5	pF	

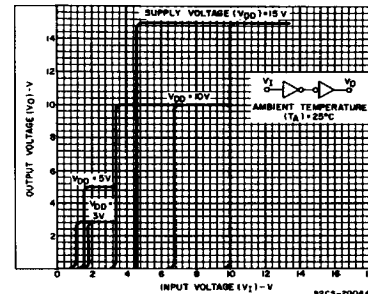


Fig. 8 - Minimum and maximum transfer characteristics - true output.

CD4041UB Types

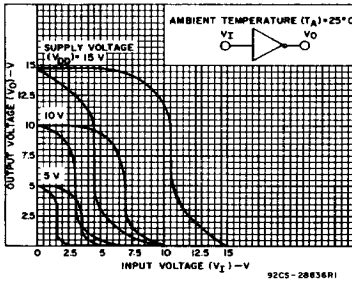


Fig. 9 - Minimum and maximum transfer characteristics - complement output.

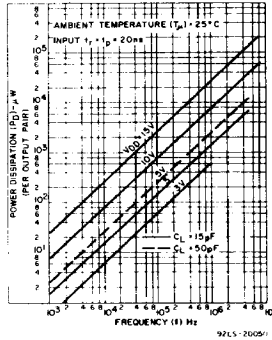


Fig. 11 - Typical power dissipation vs frequency per output pair.

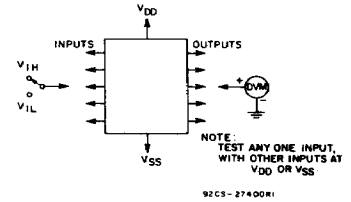


Fig. 13 - Input voltage test circuit.

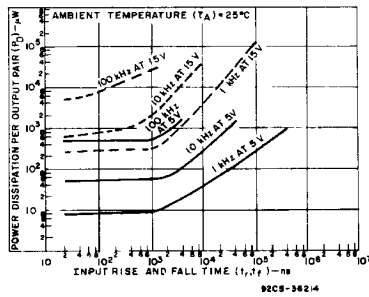


Fig. 10 - Typical power dissipation vs. input rise & fall time per output pair.

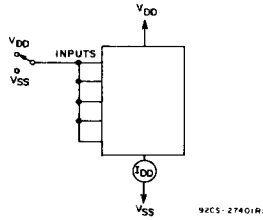


Fig. 12 - Quiescent device current test circuit.

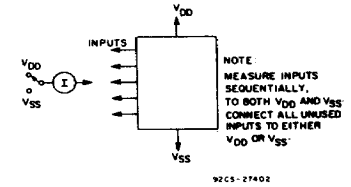
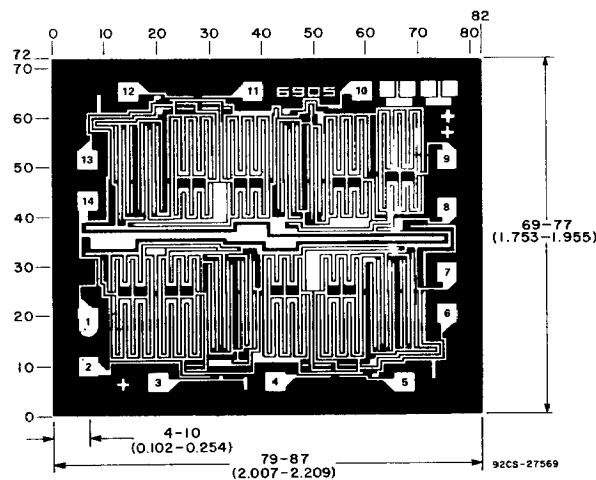


Fig. 14 - Input-leakage-current test circuit.

Dimensions and pad layout for the CD4041UBH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.